What is claimed is:

1. A semiconductor device comprising:

a substrate of a first conductivity type;

a gate structure in a plurality of trenches in the substrate, wherein in each of the trenches, the gate structure comprises a conductive gate surrounded by an insulating material that has a first thickness at a sidewall of the trench and a second thickness at a bottom of the trench, the second thickness being greater than the first thickness;

a first region of a second conductivity type adjacent to at least one of the trenches, the first region extending to a first depth in the substrate and including channel region adjacent to the trenches;

a second region of the second conductivity type, wherein the second region is in electrical contact with the first region, and the second regions extends to a second depth that is deeper than the first depth and shallower than the trenches; and

a third region of the first conductivity type atop the first region, wherein a voltage on the conductive gate control a current flow from the third region through the first region to an underlying portion of the substrate.

2. The semiconductor device of claim 1, wherein the conductive gate extends to a depth that is deeper than the first depth and shallower than the second depth.

3. The semiconductor device of claim 1, wherein the substrate comprises a first semiconductor layer atop a semiconductor substrate that is more heavily doped than the first semiconductor layer, wherein the trenches extend into the first semiconductor layer.

4. The semiconductor device of claim 3, wherein the substrate further comprises a second semiconductor layer atop the first semiconductor layer, wherein the second semiconductor layer is more lightly doped than the first semiconductor layer.

5. The semiconductor device of claim 4, wherein:

the first region forms a junction with the second semiconductor layer; and

the second region forms a junction with the first semiconductor layer.

6. The semiconductor device of claim 3, wherein the voltage on the conductive gate controls a current flow from the third region through first region and through the first semiconductor layer to the semiconductor substrate.

7. The semiconductor device of claim 1, wherein the substrate comprises a layer in which the trenches reside, the layer having a graded dopant profile such that a concentration of dopants of the first conductivity increases with depth in the layer.

8. The semiconductor device of claim 1, wherein the substrate comprises a series of implantations having varying depths and dopant concentrations such that dopant concentrations of the first conductivity increase with depth in the substrate.

9. The semiconductor device of claim 1, wherein the second region comprises a series of implantations at varying depths.

10. The semiconductor device of claim 1, wherein

the first region and the third region are in a first mesa between a first pair of the trenches; and

the second region is between a second pair of the trenches;

11. The semiconductor device of claim 10, further comprising a fourth region of the second conductivity type, wherein the fourth region is at a surface of the substrate and extends across an entire separation between the second pair of trenches.

12. The semiconductor device of claim 1, wherein a mesa between a first and a second of the trenches comprises:

the third region at a surface of the substrate and adjacent to the first trench;

a fourth region of the first conductivity type at the surface of the substrate and adjacent to the second trench;

a fifth region of the second conductivity type between the third and fourth regions at the surface of the substrate;

the first region underlying the third and fourth regions; and

the second region underlying the third region and separated from the first and second trenches.

13. The semiconductor device of claim 12, further comprising an electrical contact to the third, fourth, and fifth regions.

14. The semiconductor device of claim 1, wherein the second region extends to a first plurality of adjacent mesas that are between pairs of the trenches and is absent from a second plurality of adjacent mesas that are between pairs of the trenches.

15. The semiconductor device of claim 1, further comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the first region.

16. The semiconductor device of claim 1, further comprising a gate bus that is electrically connected to the gate structure in the trenches, wherein the gate bus overlies a portion of the substrate that includes at least part of the second region.

17. The semiconductor device of claim 1, wherein the second region has a concentration of dopants of the second conductivity type that is higher than that of the first region.

18. A fabrication process for a semiconductor device, the process comprising:

(a.) forming a plurality of trenches in a substrate of a first conductivity type;

(b.) depositing a thick oxide on bottoms of the trenches;

(c.) forming a gate oxide layer on sidewalls of the trenches;

(d.) filling the trenches with a conductive material;

(e.) forming body regions of a second conductivity in the substrate in areas corresponding to one or more mesas that are between the trenches, wherein the body regions have a first depth;

(f.) forming clamp regions of the second conductivity in areas corresponding to one or more mesas that are between the trenches, wherein the clamp regions have a second depth that is greater than the first depth but shallower than the trenches;

(g.) forming active regions of the first conductivity type above the body regions; and

(h.) providing electrical connections to the conductive material, the active regions, and the substrate.

19. The process of claim 18, wherein step (a.) is performed before steps (e.) and (f.).

20. The process of claim 18, wherein steps (e.) and (f.) is performed before step (a.).

21. The process of claim 18, further comprising patterning the conductive material to form a gate bus overlying the substrate.

22. The process of claim 21, wherein forming the body regions comprises implanting dopants of the second impurity type through the gate bus.

23. The process of claim 21, wherein forming the clamp regions comprises implanting dopants of the second impurity type through the gate bus.

24. The process of claim 18, further comprising:

removing the conductive material from a surface of the substrate; and

forming a gate bus that contacts the conductive material and overlies portions of the substrate, wherein

forming the body regions and the clamp regions occurs after removing the conductive material from a surface of the substrate and before forming the gate bus.

25. The process of claim 18, wherein each of the trenches crosses one or more of the other trenches.